Application Note_PNDM12P204A1: Dual Channel Isolated Gate Driver for PNJ´s 62mm Half-Bridge SiC Module

About this document

This document is prepared as an application note of how to design a proper gate driver for PN Junction Semiconductor（PNJ）´s 62mm half-bridge SiC module with miller clamp and DESAT protection functions. The reference board is available for designers to carry out double pulse test or driver circuit design based on PNJ's 62mm half-bridge SiC module.

Demo Product Name: PNDM12P204A1
PN Junction Semiconductor (PNJ) Co., Ltd
PNJ Application Team

The Evaluation and Reference Boards are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document.

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1 Introduction

The purpose of this document is to demonstrate the high performance of PNJ´s 62mm half-bridge SiC module and provides a matched gate driver reference design. The PNDM12P204A1 gate driver board, shown in Figure 1, offers reliable connection between driver and 62mm half-bridge SiC module.

Technical features:

1) Optimized for PNJ´s high-performance PAA12400BM3 SiC module
2) High-frequency, ultra-fast switching
3) On-board 2.5 W isolated power supplies with UVLO protections
4) Adjustable voltage level for both turn-on and turn-off
5) UVLO protections with hysteresis
6) ±10A pulse current capability with split outputs
7) 150-V/ns minimum CMTI
8) Fast DESAT protection up to 200 ns response time
9) 4-A Internal active miller clamp circuit
10) Isolated analog sensor with PWM output for temperature sensing

Fig. 1. 62mm half-bridge SiC module PAA12400BM3 and PNDM12P204A1

2 Board Overview

2.1 Structure of PNDM12P204A1

Figure 2 shows the structure of the gate driver board. The board is divided into three parts by insulation barrier, which are the primary side, the high-side gate driver and the low-side gate driver. The board is powered by a single 12V DC power supply at the primary side. A 14-pin IDC connector which includes power pins, PWM signals and fault signals is placed at the primary side. The high-side gate driver and low-side gate driver are powered by two isolated power supplies based on Texas Instruments´s LM5180. The transformers used in the isolated power supply can achieve 4000VAC isolation. The gate driver adopts Texas Instruments´s UCC21750, which is an isolated gate driver IC with miller clamp, desaturation detection and isolated temperature sensing functions. The isolation voltage for UCC21570 is 2121VDC. The pin description of the 14-pin IDC connector is shown in Table 1.

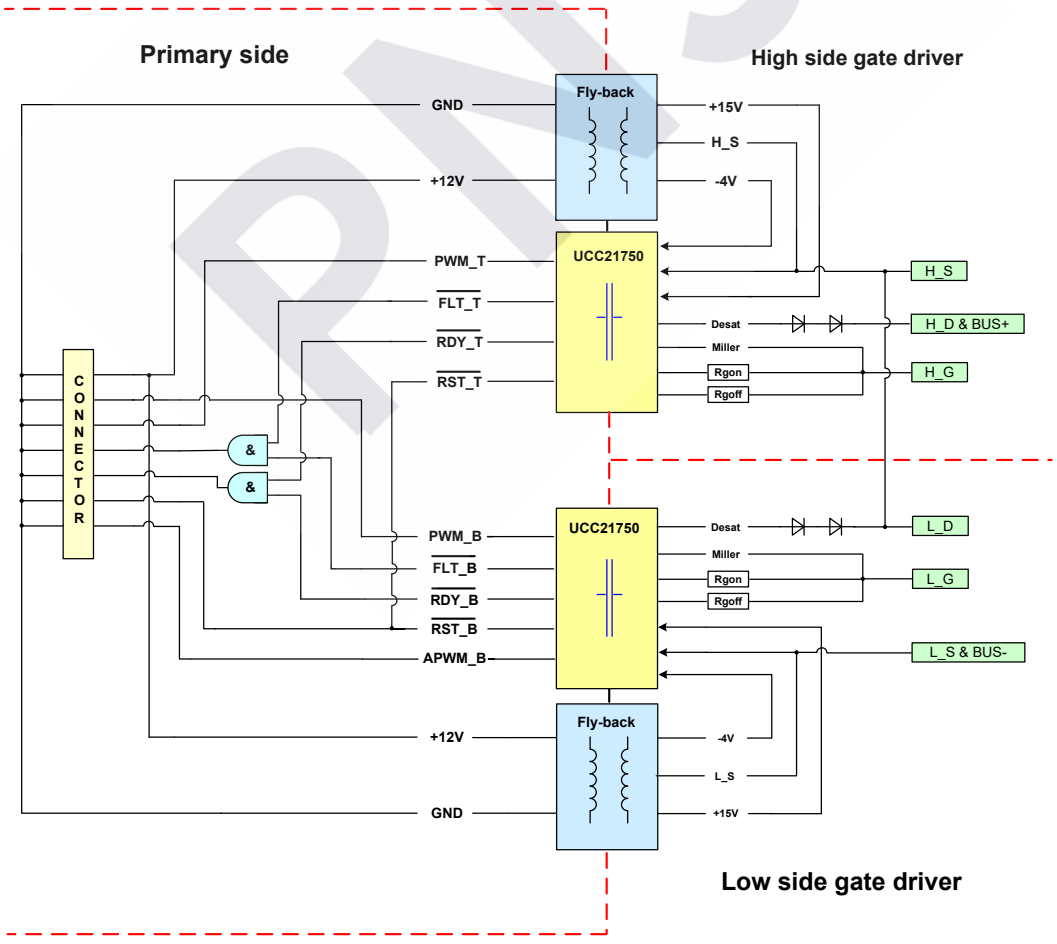

Fig. 2 Structure of PNDM12P204A1

Table 1 Pin description

Pin	Name	I/O	Description
1	GND	G	ground
2	VDD	P	power supply input pin (+12 V nominal input)
3	GND	G	ground
4	IN_PWM_B	I	low-side PWM input
5	GND	G	ground
6	IN_PWM_T	I	high-side PWM input
7	GND	G	ground
8	FLT	O	over current or short circuit fault signal
9	GND	G	ground
10	RDY	O	power ready and fault for UCC21750
11	GND	G	ground
12	IN_RST	I	when a fault exists, bring this pin low to clear the fault
13	GND	G	ground
14	AD_TEMP	O	temperature sensing signal

P = Power, G = Ground, I = Input, O = Output

2.2 Physical Dimensions and Pinouts

Physical dimensions and pinouts of PNJ's PNDM12P204A1 Gate Driver Board are shown in Figure 3 and Figure 4. The board' s size is 68mm x60m x 31mm.

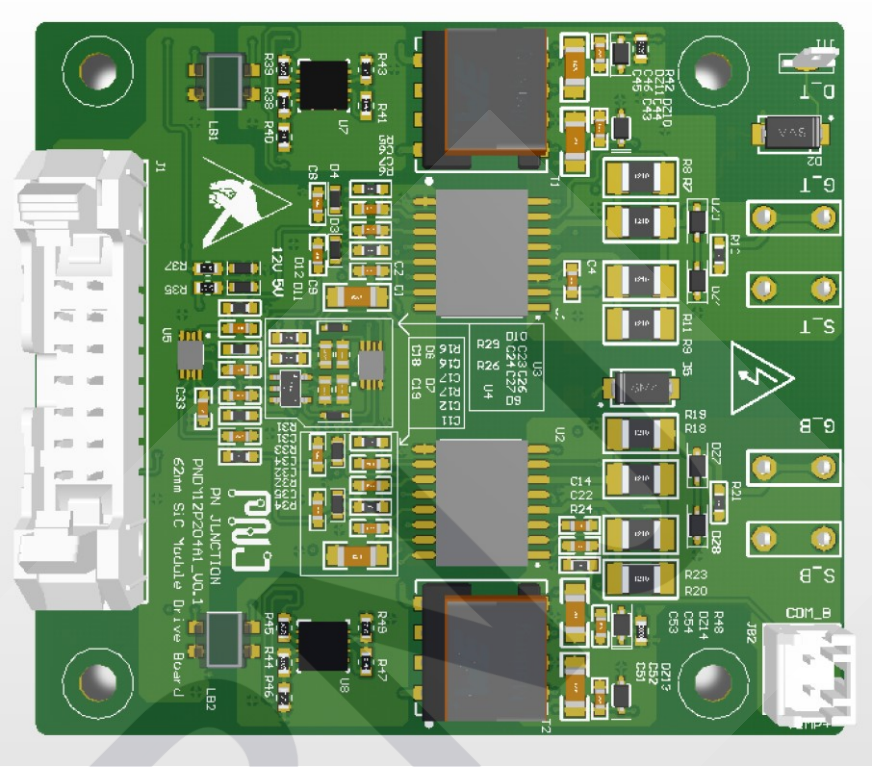

Fig. 3 Top View of PNJ's PNDM12P204A1

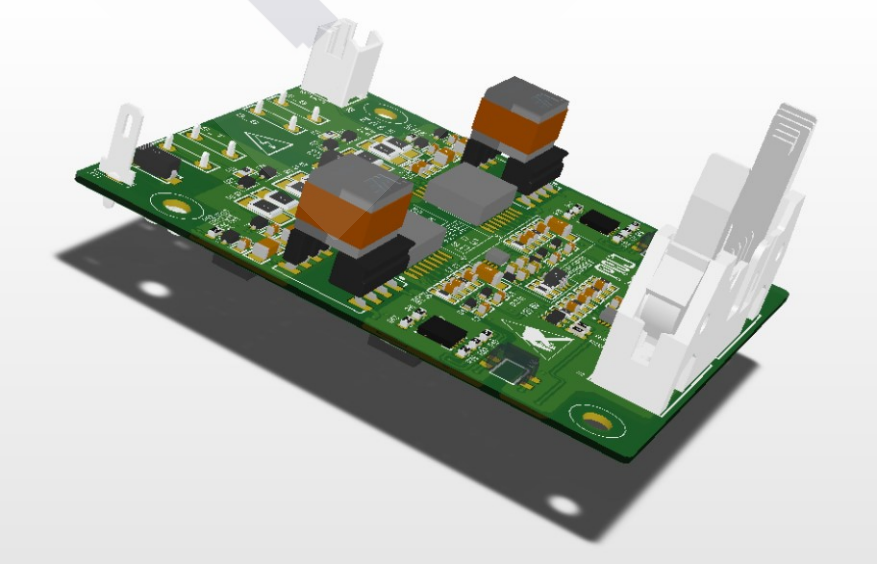

Fig. 4 Front View of PNJ's PNDM12P204A1

3 PNDM12P204A1 Hardware

3.1 Schematic

The schematic of PNDM12P204A1 is shown in Figure 5-8.

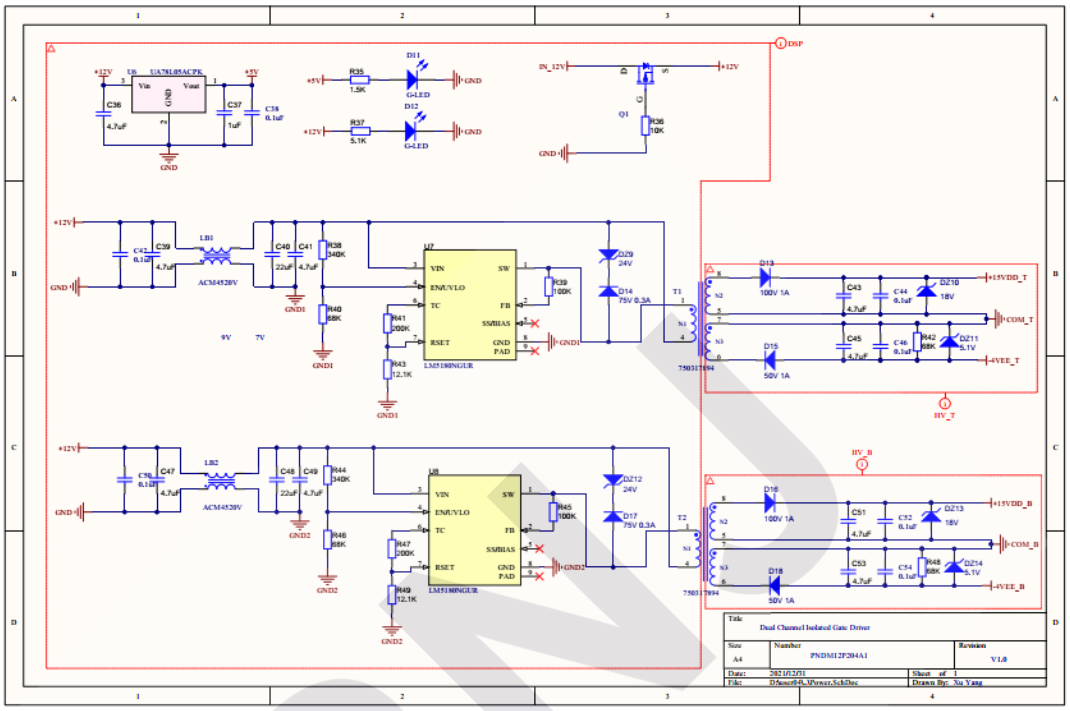

Fig. 5 Schematic of PNDM12P204A1 Page1

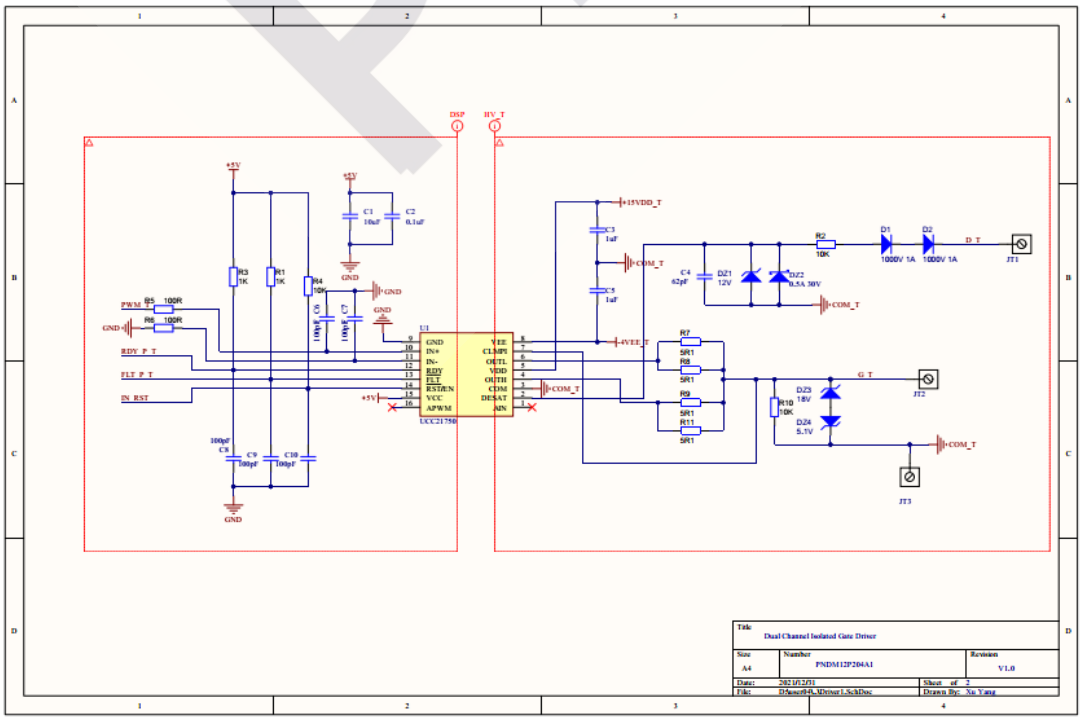

Fig. 6 Schematic of PNDM12P204A1 Page2

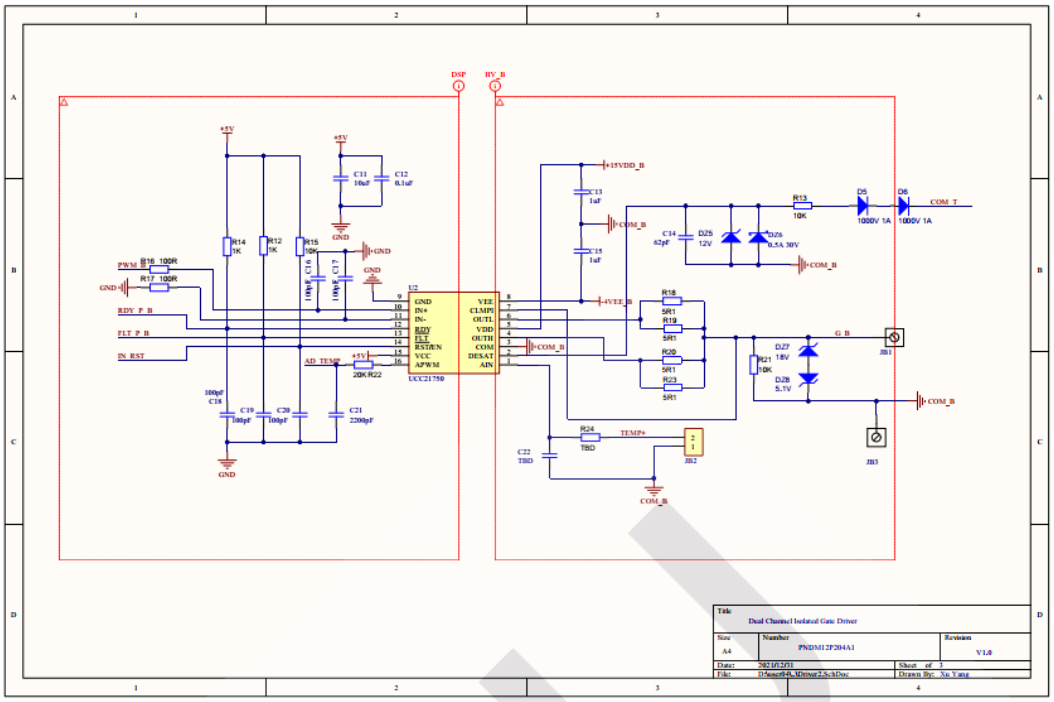

Fig. 7 Schematic of PNDM12P204A1 Page3

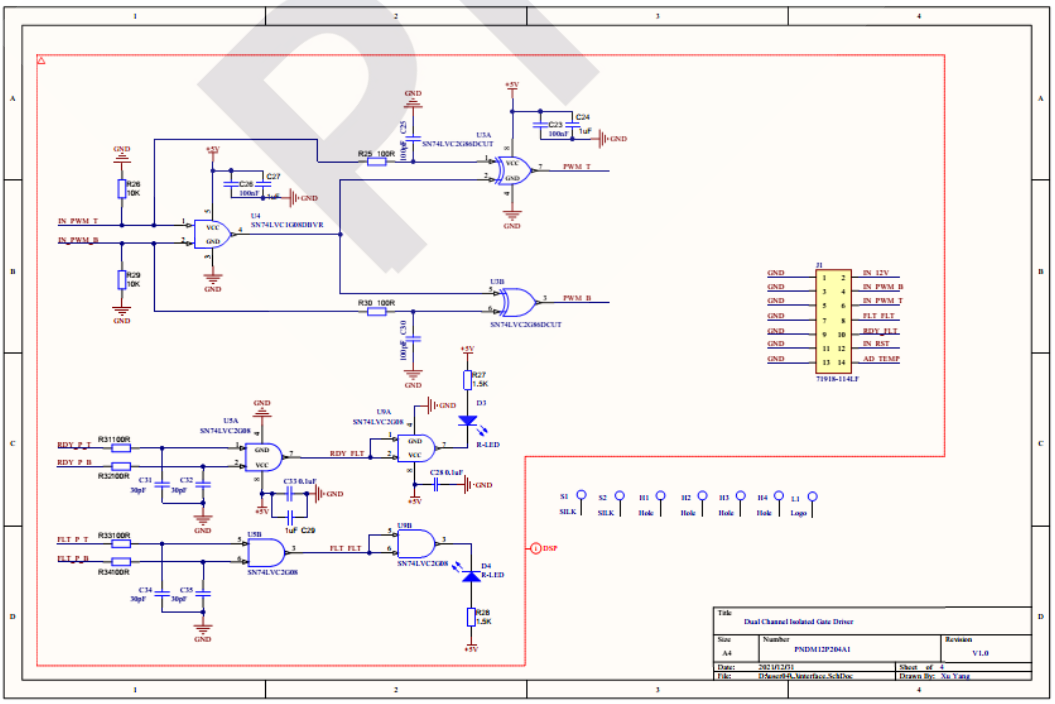

Fig. 8 Schematic of PNDM12P204A1 Page4

3.2 Layout

The layout of PNDM12P204A1 is shown in Figure 9-12.

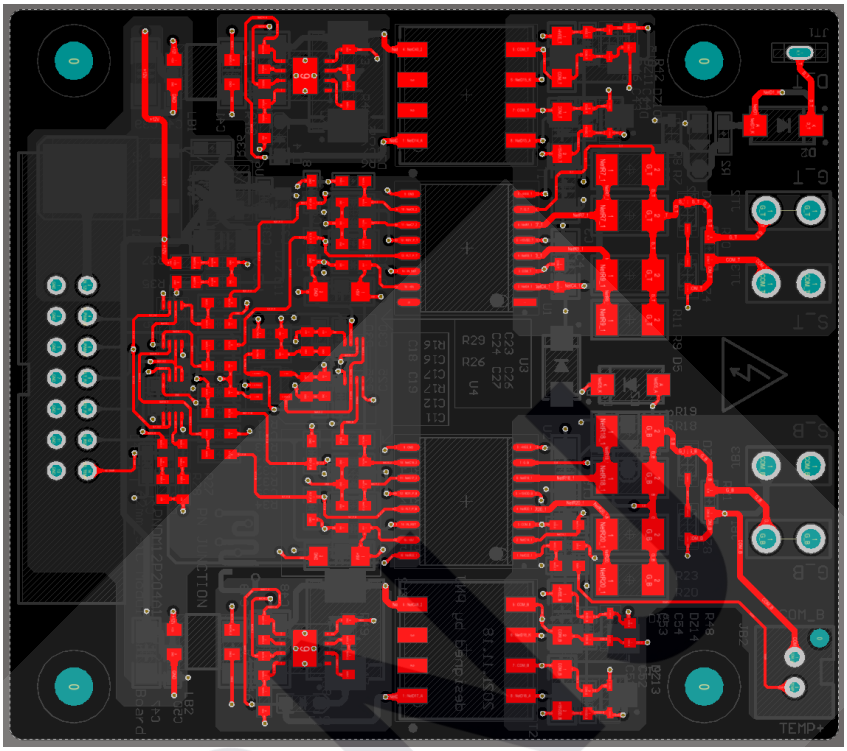

Fig.9 Top layer

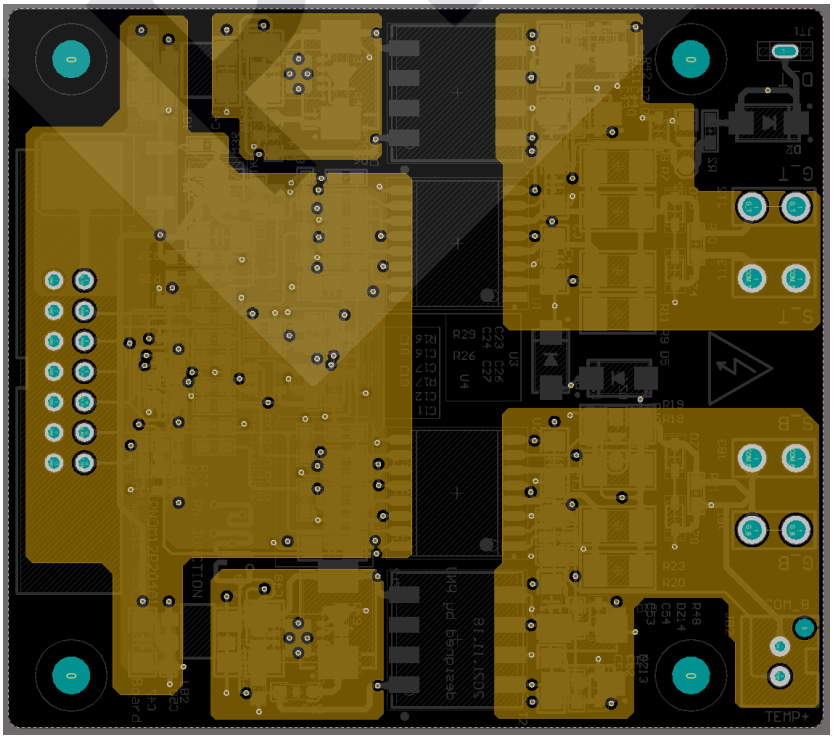

Fig.11 Inner layer 1

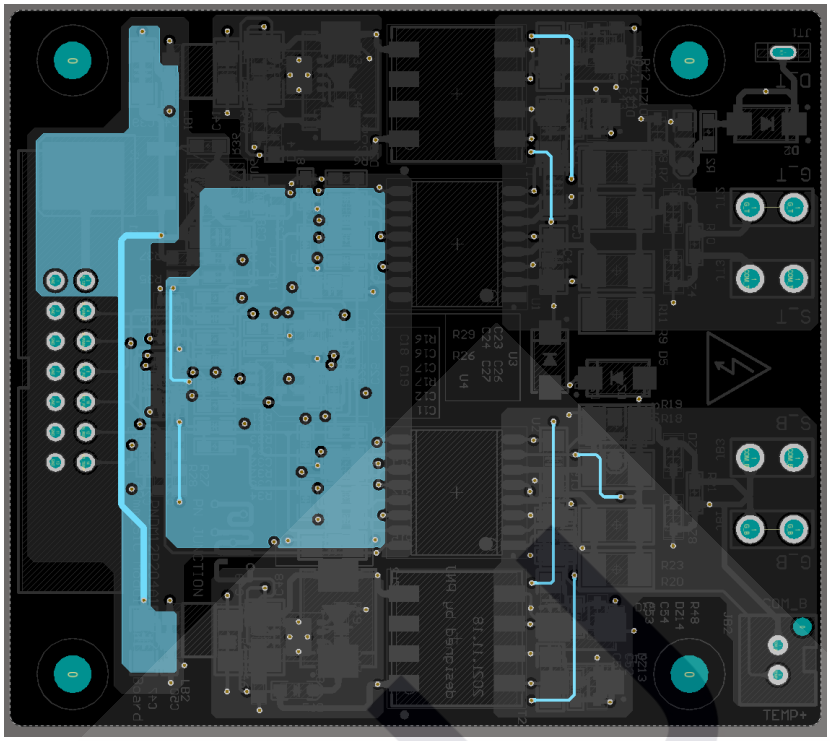

Fig.12 Inner layer 2

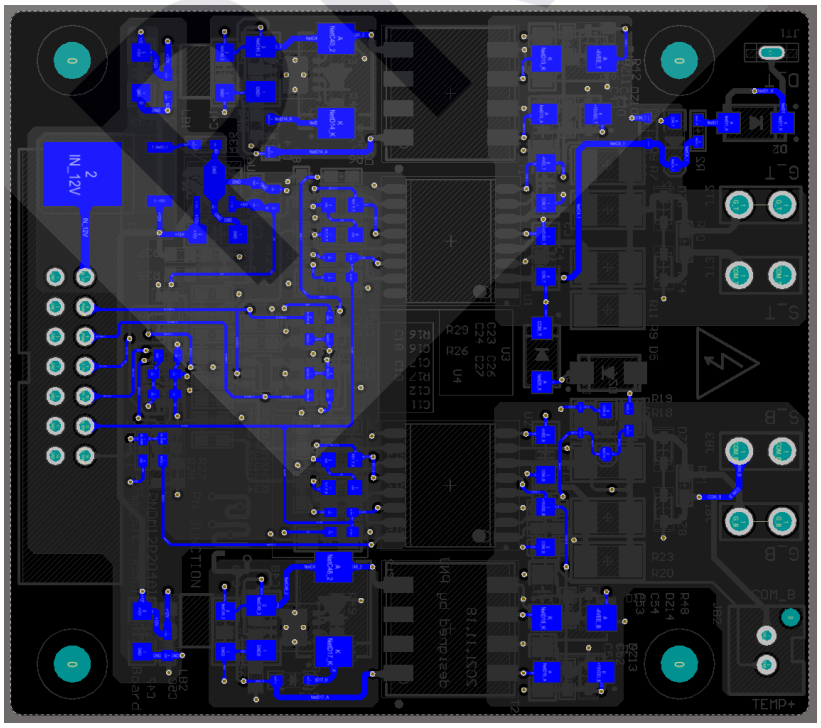

Fig.13 Bottom layer

3.3 Bill of Material (BOM)

BOM of PNDM12P204A1 is shown in Tab 2.

Tab.2 BOM of PNDM12P204A1

Manufacturer P/N	Manufacturer	Description	Designator	Quantity
CC0603FRNPO9BN620	Yageo	CFCAP X7R S 62pF 50V 0603 belt	C4, C14	2
CC0603KPX7R9BB101	Yageo	CFCAP X7R S 100pF 50V 0603 belt	C6, C7, C8, C9, C10, C16, C17, C18, C19, C20, C25, C30	12
CC0603KPX7R9BB222	Yageo	CFCAP X7R S 2200pF 50V 0603 belt	C21	1
CC0603KRX7R8BB104	Yageo	CAP X7R S 100nF 25V 0603_H9 belt	C23, C26	2
CC0603KRX5R8BB105	Yageo	MLCC_SMD/SMT 0603 25Vdc 1 uF X7R 10%	C24, C27, C29, C37	4
CC0603FRNPO9BN300	Yageo	CFCAP X7R S 30pF 50V 0603 belt	C31, C32, C34, C35	4
CC0603KRX7R8BB104	Yageo	CFCAP X7R S 0.1uF 25V 0603 belt	C2, C12, C28, C33, C38, C42, C44, C46, C50, C52, C54	11
CC1206KKX5R7BB106	Yageo	CFCAP X7R S 10uF 16V 1206 belt	C1, C11	2
C3216X7R1H105K160AB	TDK	CFCAP X7R S 1μF 50V 1206_H14 belt	C3, C5, C13, C15	4
CC1206KKX5R9BB475	Yageo	MLCC_SMD/SMT 1206 50Vdc 4.7uF X7R 10%	C36, C39, C41, C43, C45, C47, C49, C51, C53	9
12103D226MAT2A	AVX	MLCC_SMD/SMT 1210 25Vdc 22uF X7R 20%	C40, C48	2
RT0603FRD07100RL	Yageo	RES SMD 100R 1% 1/10W 0603	R5, R6, R16, R17, R25, R30, R31, R32, R33, R34	10
RT0603FRE0710KL	Yageo	RES SMD 10K 1% 1/10W 0603	R2, R4, R10, R13, R15, R21, R26, R29, R36	9
RT0603FRE0720KL	Yageo	RES SMD 20K 1% 1/10W 0603	R22	1
AC0603FR-071K5L	Yageo	RES SMD 1.5K 1% 1/10W 0603_H6	R27, R28, R35	3
RC0603FR-075K1L	Yageo	RES SMD 5.1K OHM 1% 1/10W 0603_H6	R37	1
AC0603FR-07340KL	Yageo	RES SMD 340K OHM 1% 1/10W 0603	R38, R44	2
RC0603FR-07100KL	Yageo	RES SMD 100K OHM 1% 1/10W 0603	R39, R45	2
AC0603FR-1068KL	Yageo	RES SMD 68K OHM 1% 1/10W 0603	R40, R42, R46, R48	4
RT0603FRE07200KL	Yageo	RES SMD 200K OHM 1% 1/10W 0603	R41, R47	2
RC0805FR-071KL	Yageo	RES SMD 1K 1% 1/8W 0805	R1, R3, R12, R14	4
RC1210FR-075R1L	Yageo	RES SMD 5.1 OHM 1% 1/2W 1210	R7, R8, R9, R11, R18, R19, R20, R23	8
RN73H1JTTD1212D25	KOA speer	RES SMD 12.1K OHM 0.5% 1/10W 0603_H6	R43, R49	2
RS1MDF-13	Diode incorporated	Diode 1000V 1A RS1MDF-13	D1, D2, D5, D6	4
15M-LTST-C191KRKT	liteon	LED S red If=30mA,VF=2V,15M-LTST-C191KRKT	D3, D4	2
21M-LTST-C190KGKT	liteon	LED S green If=30mA,VF=2V,21M-LTST-C190KGKT	D11, D12	2
B1100Q-13-F	Diode incorporated	Diode 100V 1A B1100Q-13-F	D13, D16	2
BAV16WS-7-F	Diode incorporated	Diode 75V 0.3A BAV16WS-7-F	D14, D17	2
B150B-13-F	Diode incorporated	Diode 50V 1A BB150B-13-F	D15, D18	2
BZX84J-B12,115	Nexperia	Z-DIO S 12V.BZX84J-B12V belt	DZ1, DZ5	2
BAT42W-TP	MCC	Z-DIO S 30V BAT42W-TP belt	DZ2, DZ6	2
BZX84J-B18,115	Nexperia	Z-DIO S 18V.BZX84J-B18 115 belt	DZ3, DZ7, DZ10, DZ13	4
BZX84J-B5V1,115	Nexperia	Z-DIO S 5.1V.BZX84J-B5V1 belt	DZ4, DZ8, DZ11, DZ14	4
SML4749AHE3_A/H	Vishay	DO-214AC 24V SML4749AHE3_A/Hbelt	DZ9, DZ12	2
71918-114LF	Amphenol FCI	71918-114LF	J1	1
3534	Keystone	M5 SCREW MNT TERMINAL,30A	JB1, JB3, JT2, JT3	4
1376478-2	TE	2P_1376478-2	JB2	1
8196	Keystone	M5 SCREW MNT TERMINAL,30A	JT1	1
ACM4520V-231-2P-T00	TDK	Common chock_230R@100MHZ,1.5A/50V,ACM4520V	LB1, LB2	2
ZXMP7A17KTC	Diodes Incorporated	P-MOS ZXMP7A17KTC 70V 5.7A	Q1	1
WE-AGDT_EP7	Wurth Elektronik	WE-AGDT Auxiliary Gate Drive Transformer, EP7, SMT, 9-18Vin, 15/4Vout, 3Wout	T1, T2	2
UCC21750QDWQ1	TI	UCC21750	U1, U2	2
SN74LVC2G86DCUT	TI	Dual 2-input Exclusive-OR Gate	U3	1
SN74LVC1G08DBVR	TI	SN74LVC1G08DBVR	U4	1
SN74LVC2G08DCUT	TI	SN74LVC2G08DCUT	U5, U9	2
UA78L05ACPK	TI	IC REG LINEAR 5V 100MA SOT89-3	U6	1
LM5180NGUR	TI	LM5180NGUR	U7, U8	2

4 Detailed Description

4.1 Maximum Ratings

The maximum ratings of PNDM12P204A1 are shown in Table 3

Table 3 The maximum ratings of PNDM12P204A1

Symbol	Parameter	Value	Unit
V_{dc}	Supply voltage	±18	V
I_o	Output peak current (TA = 25 °C)	±10	A
P_{drive}	Output power per channel (TA = 25 °C)	2.5	W
T_{op}	Ambient operating temperature	-40~85	℃
T_{stg}	Storage temperature	-40~125	

The switching frequency of the driver board is limited by the maximum output power of the driver' s power supply. The power loss of the gate driver depends on SiC MOSFET' s Qiss, gate voltage magnitude and the switching frequency. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the power supplies datasheet.

The total power consumption for each gate driver circuit (high-side or low-side) can be calculated by the following equation.

$$P_{DRI} = Q_G * F_S * \Delta V_{OUT}$$

P_{DRI} : gate driver power consumption (per channel)

Q_G : total gate charge (per channel)

F_S : switching frequency

ΔV_{OUT} : voltage magnitude at the driver output

Example:

Calculate the maximum switching frequency for PNDM12P204A1

P_{DRI} : 2.5 W (rated output power of isolated power supply on gate driver)

Q_G : 940 nC

$F_{S\text{-}max}$: Maximum switching frequency

ΔV_{OUT} : 25V

$$F_{s-max} = \frac{P_{DRI}}{Q_G * \Delta V_{OUT}} = \frac{2.5W}{940nC * 25V} \approx 85kHz$$

$F_{S\text{-}Max}$ ≈ 85 kHz with margin

4.2 Gate Driver Electrical Characterization

The gate driver electrical characteristics is shown in Table 4

Table 4 The gate driver electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DC}	Supply voltage	9	12	18	V	
V_{DCUVLO}	Enable threshold		9			turn on, voltage going high
	Standby Threshold		7			under voltage lockout
	UVLO hysteresis		2			
V_{IH}	High level logic input voltage	3.5		5.5		CMOS inputs
V_{IL}	Low level logic input voltage			1.5		
$V_{GATE,HIGH}$	High level output voltage		15/20			referenced to source
$V_{GATE,LOW}$	Low level output voltage		-4/-5			
V_{IOWM}	Working isolation AC (sine wave) voltage		1500			
	Working isolation DC voltage		2121			
C_{ISO}	Isolation capacitance		1		pF	UCC21750 per channel
CMTI	Common mode transient immunity		150		V/nS	
$R_{G\ IC-ON}$	Output pull-up resistance		2.5		Ω	I_{OUT}=0.1A
$R_{G\ IC-OFF}$	Output pull-down resistance		0.3			
$R_{G\ EXT-ON}$	External turn-on resistance		2.55			external SMD resistor 1210
$R_{G\ EXT-OFF}$	External turn-off resistance		2.55			
t_{ON}	Output rise time		33		nS	

t_{OFF}	Output fall time		27			R_{G-Ext} = 0 Ω C_{Load} = 100pF from 10% to 90%
t_{PHL}	Propagation delay (turn off)	60	90	130		R_{G-Ext} = 0 Ω C_{Load} = 10 nF
t_{PHL}	Propagation delay (turn on)	60	90	130		
t_{Blank}	Over-current blanking time		200			R_{G-Ext} = 0 Ω C_{Load} = 100pF
$t_{PD-FAULT}$	Over-current propagation delay to FAULT signal low	400	580	750		
t_{ss}	Soft-shutdown time			3	uS	
I_{STO}	Soft turn-off current on fault conditions	250	400	570	mA	
R_{MC}	Miller clamp resistance		0.6		Ω	I_{CLMPI} = 0.2A
V_{MC}	Miller clamp voltage threshold	1.5	2	2.5	V	reference to V_{EE}
f_{APWM}	APWM output frequency	300	400	420	kHZ	V_{AIN}=2.5V

4.3 Function Descriptions

Fault signal:

The driver board has two fault signals, FLT signal and RDY signal.

FLT signal:

When the driver IC detects that the DESAT voltage is higher than the user defined threshold, the PWM signals will be turned off immediately. Meanwhile, the FLT signal will be pulled down and the FLT signal pin in connector J1 is pulled low too.

RDY signal:

After the board is powered on, the driver IC will monitor the voltage of the primary side power supply VCC and the secondary side power supply VDD. If an undervoltage event is detected in any one of them, the driver IC will pull the RDY pin low and the RDY signal pin of the corresponding connector is pulled low too.

RST signal:

When the driver IC is in DESAT protect condition, the FLT signal is pulled low. This signal cannot be self-recovered and needs to be cleared by pulling the RST signal low for 1us.

Undervoltage protection:

There are two undervoltage protections on board for the flyback converter and the driver chip UCC21750 respectively. The flyback converter undervoltage protection is set to 9V. The primary side undervoltage protection value of the drive chip is 2.5V (0.2V hysteresis voltage) and the secondary side undervoltage protection value is 10.7V (0.8V hysteresis voltage).

DESAT protection:

When an over-current or short-circuit condition in the circuit causes V_{DS} to rise during on-state, the V_{DS} voltage is detected and compared with an internal comparator reference voltage 9.15V in the driver chip. When DESAT voltage reaches above the threshold value, the driver chip will immediately turn off the PWM signal to prevent the module from being damaged.

AD sampling:

When the inverter is working, it is often necessary to collect the bus voltage and module temperature. The driver chip can provide a channel of isolated voltage signal sampling, and output the collected voltage signal at a fixed frequency of 400KHZ. The output will have a different duty cycle if the voltage is different. The voltage and duty cycle satisfy the following equation

$$D_{APWM}(\%) = -20 * V_{AIN} + 100$$

V_{AIN}: driver chip AIN pin voltage

Input power anti-reverse connection:

In order to prevent the input power from damaging the driver board, the driver incorporates a reverse connection protection circuit shown in previous schematics.

4.4 Truth Table

The corresponding PWM input and output under different pin states of the driver chip are shown in Tab 5.

Tab.5 The truth table of PNDM12P204A1

PWM	RST	DESAT FLT	RDY FLT	OUTPUT
H	L	H	H	H
L	L	H	H	L
X	L	L	H	L
X	L	H	L	L

4.5 Adjustable Output Voltage

The schematic of the isolated power supply for the gate driver circuit is shown in Fig 14.

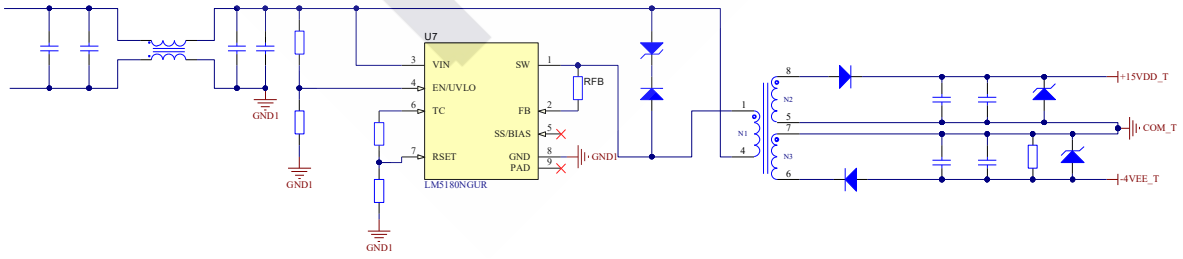

Fig.14 Isolated power supply circuit for gate driver circuit

The output voltage can be adjusted by adjusting the resistor' s value of R_{FB}. The corresponding relationship between R_{FB} and V_{OUT} satisfies the following equation:

$$R_{FB} = \frac{(V_{OUT} + V_D) * N_{PS}}{0.1mA}$$

V_{OUT}: The output voltage of turn-on voltage level(+15V is the in this design)

V_D: Secondary side diode' s forward bias voltage drop

N_{PS}: Transformer' s turns ratio

The transformer´s turns ratio is N_P:N_{S1}:N_{S2}=2.25:3.5:1, The winding configuration is shown in Fig15.

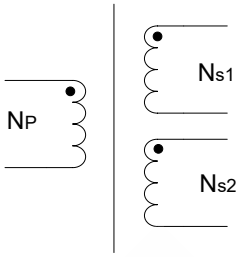

Fig.15 the transformer' s schematic diagram

The main driving voltages of SiC MOSFET are +15/-3V and +20/-5V. The driver is conventionally set to +15/-4V to drive the SiC MOSFET. It can be changed +20/-5V driving voltage to fit other applications by changing the R_{FB} from the original 100K resistor to 130K resistor and removing the zener diode (the specification is +18V zener).

4.6 Over-Current Trip Level

The gate driver implements a fast overcurrent and short circuit protection feature to protect the SiC module from catastrophic breakdown during fault. The DESAT pin of the device has a typical 9.15V threshold with respect to COM, source or emitter of the power semiconductor. The typical value of the internal current source is 500μA. The principle of desaturation circuit is shown in Figure 16. The voltage on the DESAT pin of the chip satisfies the following equation.

$$V_{DESAT} = V_{RDESAT} + 2V_F + V_{DS} = 500uA + 2 * 0.83V + V_{DS}$$

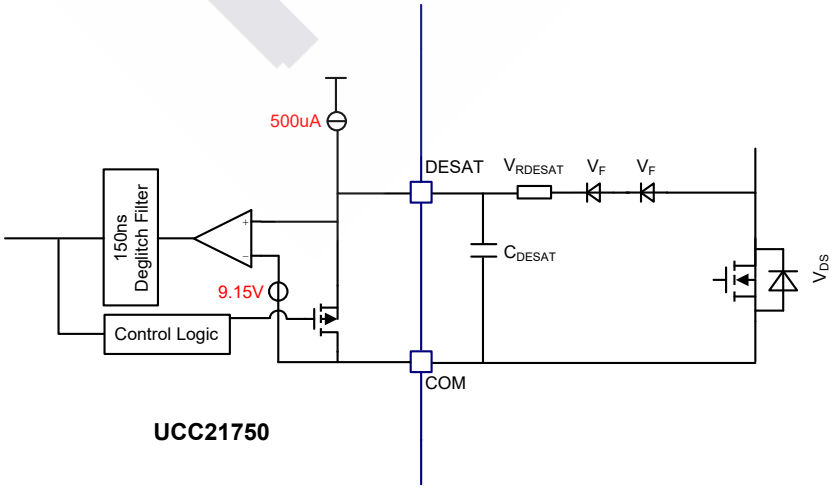

Fig.16 desaturation protection circuit

The required overcurrent protection point can be adjusted by the value of the

resistor R_{DESAT}. Since the V_{DS} of the power switch device varies greatly and the overcurrent protection relies on the detection of V_{DS}, the DESAT threshold should be set to a conservative value to avoid premature triggering. By choosing different C_{DESAT} capacitors, the blanking time can be set, and the blanking time can be calculated with the following equation

$$t_{BLK} = \frac{C_{DESAT} * 9.15V}{500uA}$$

Typically, setting the blanking time to 1~2us should be enough to prevent the DESAT protection circuit from malfunctioning.

To select an appropriate over-current trip threshold, refer to the I_D vs V_{DS} output characteristic curves in the PAA12400BM3' s datasheet. The over-current fault condition must be cleared by the reset signal to return to normal operation.

5. Revision History

Date	Revision	Description of change
2022.01.11	V1.0	Initial Version